HIGH VOLTAGE MOSGATED DEVICE WITH TRENCHES TO REDUCE ON-RESISTANCE

CROSS REFERENCE TO RELATED APPLICATION

This application is based on and claims priority to U.S. Provisional Patent Application No. 60/113,641, filed Dec. 23, 1998, the entire disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

This invention relates to MOSgated devices and more specifically relates to a novel super junction-type device and method for its manufacture, which has a low on-resistance and high breakdown voltage.

MOSgated devices such as power MOSFETs, IGBTs, and gate turn on thyristors are well known. A typical MOSgated device of this type is shown in U.S. Pat. No. 5,007,725. These devices may be made with a closed cellular base or spaced striped base topology. A device termed a COOLFET device made by Siemens Corporation, consists of a device in which spaced trenches form small width areas of increased conductivity epitaxially formed silicon. The higher conductivity epi reduces on-resistance, but is depleted under blocking voltage conditions to provide a high breakdown voltage. Such devices, termed superjunctions, are described in U.S. Pat. Nos. 4,754,310 and 5,216,275. This invention provides an improved device of the COOLFET type in which simpler manufacturing and improved operation is provided.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the invention, a semi-insulating material, preferably a semi-insulating polysilicon or other non-injecting material fills vertically oriented parallel spaced trenches which extend completely through a depletable epitaxial silicon layer and reach, or are closely spaced from, the conductive silicon substrate which supports the epitaxial layer. The trenches could be lined with highly insulative silicon dioxide (to prevent injection) and then filled with conventional conductive polysilicon. A similar structure is used in termination of the chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-section of the active portion of a semiconductor chip which uses the present invention.

FIG. **2** is a portion of the trench of FIG. **1** which has a modified structure.

FIG. **3** is a cross-section of the termination portion of the chip of FIGS. **1** and **2**.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-section of the active area of a high voltage vertical conduction D-MOS device made in accordance with the invention. While any suitable topology can be used, the embodiment of FIG. **1** is carried out with a parallel spaced stripe design as will be later described.

A significant portion of the on-resistance R_{DSON} of prior art devices is produced in the N^- epitaxial layer (for an N channel device). The thickness and resistivity of this layer is chosen to meet the breakdown voltage of the device. Thus, the higher the breakdown voltage is to be, the greater the thickness and the higher the resistivity. Both conditions increase the device R_{DSON}.

The present invention permits the use of a lower resistivity N^- epi layer for a given breakdown voltage, thus reducing R_{DSON} for a given breakdown voltage.

Referring to FIG. **1**, there is shown a portion of a MOSgated chip **10** which consists of an N^+ silicon substrate **11** which has an N^- epitaxially grown junction-receiving silicon layer **12** thereon. The thickness and resistivity of N^- layer **12** is chosen in accordance with the desired breakdown voltage of the device to be formed. The invention is described herein for an N channel device. The invention can be employed in a P channel device by reversing all concentration types.

Elongated parallel base diffusion strips **15**, **16**, **17** and **18** are formed in the top surface of layer **12** by any suitable well known photolithographic process. A typical process will include the opening of elongated windows in a masking layer (which may include a poly-silicon gate and underlying gate oxide), the implant of a suitable P type impurity such as boron and the subsequent diffusion of the impurity. N^+ source regions **20** to **25** are next formed as spaced pairs in each of the P regions **15** to **18** to form invertible channels along the opposite edges of each of bases **15** to **18**. These invertible channels are covered by MOSgates consisting of gate insulation layers (preferably silicon dioxide) **30** to **32** covered by conductive polysilicon gate electrodes **33** to **35** respectively. Gate electrodes are then covered by insulation layers (LTO) **36** to **38** respectively which insulates the gates from the overlying source electrode **39**. A drain electrode **40** is applied to the bottom of substrate **11**.

The structure of FIG. **1** described to this point is that of a conventional planar stripped geometry MOSFET of the kind shown in pending application serial No. 60/107,700, filed Nov. 9, 1998, the disclosure of which is incorporated herein by reference. In accordance with the invention, vertical trenches **49**, **50**, **51** are cut at least partly through the epi layer **12** and bisect each of the base strips **16** and **17**, and all other base strips. FIG. **1** shows trenches **50** and **51** as ending just short of the full thickness of epi layer **12**, but they can extend to reach the N^+ layer **11** as shown in dotted lines. These trenches **49**, **50** and **51** are then filled with fillers **48**, **52** and **53** respectively, of high resistivity, non-injecting material, preferably SIPOS which is a semi-insulation polysilicon. SIPOS can be formed by adding oxygen during the deposition of polysilicon fillers **48**, **52** and **53**. The addition of oxygen during this process changes the character of the polysilicon from a semiconductor to an insulation, as is known in the art.

The trenches **49**, **50** and **51** are made as thin as possible to reduce leakage current during operation. For example, a trench width of 1 micron is acceptable, although larger widths are permissible and smaller widths are desirable.

The depth of the trenches **49**, **50** and **51** will depend on the thickness of epi layer **11**, and may be about 40 microns for a device having a 400 to 500 volt breakdown. While any desired wafer structure (in which a large number of chips are simultaneously formed), the ultra-thin wafer described in U.S. Pat. No. 5,549,762 (Cantarini) is well adapted for use with the present invention.

The novel structure of FIG. **1** allows the use of a lower resistivity for epi **12** for a given breakdown voltage. The trenches **49**, **50** and **51** are spaced close enough that the lateral field during a blocking condition will deplete electrons from the N^- epi between trenches, holding the transistor off. The resistivity of the SIPOS fillers **48**, **52** and **53** is chosen to provide this lateral field without excessive current leakage. During forward conduction of the device, the lower resistivity of the epi **12** reduces the R_{DSON} of the device.

FIG. **2** shows a second embodiment of the invention in which elements similar to those of FIG. **1** have the same